COMMENTS

No claims are amended, no claims are canceled, and no claims are added; as a result, claims 5-8 and 29-71 remain pending in this application.

Double Patenting Rejection

Claims 5-8 and 29-71 were provisionally rejected under the judicially created doctrine of double patenting over claims 1-4, 26-28, and 32-57 of U.S. Application Serial No. 08/886,753. Applicant notes that U.S. Application Serial No. 08/886,753 issued as U.S. Patent No. 6,286,062. Applicant further notes that the judicially created doctrine of double patenting can be overcome by filing a terminal disclaimer. Applicant will await allowance of the present claims prior to considering whether to file a terminal disclaimer or whether to traverse this rejection.

§112 Rejection of the Claims

Claims 5-8 and 29-71 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. More particularly, the Office Action states that

> There is no mention in the specification of several critical features of the claims, specifically, that "each memory device contains a data in and data out buffer, a column decoder and a row decoder".

Applicant respectfully traverses. The specification contains numerous references to embodiments of the present invention that include DRAM as the memory device. Applicant attaches two figures from *DRAM Circuit Design*, by Brent Keeth and R. Jacob Baker, I.E.E.E. 2001. Each figure shows a DRAM circuit that contains a data buffer, a column decoder and a row decoder. Accordingly, one of ordinary skill in the art would find the data in and data out buffer, column decoder and row decoder as recited in the claims to be sufficiently described to enable the one of ordinary skill in the art to make and/or use the invention. Withdrawal of the § 112, first paragraph rejection is respectfully requested.

§103 Rejection of the Claims

Claims 5-8 and 29-71 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Katayama et al. (U.S. Patent No. 5,875,452). Applicant respectfully traverses.

The Examiner, in rejecting claims 5-8 and 29-71, states that Katayama teaches the claimed invention in a memory system comprising a memory controller with a unidirectional command and address bus, a bidirectional data bus, a plurality of memory devices, such as eight, a shared command buffer coupled between the command and address bus and the plurality of memory devices for receiving and latching commands and addresses, a shared data buffer connected between the plurality of memory devices and the bidirectional data bus for receiving and latching read data or write data. In addition, the Examiner states that Katayama teaches the claimed pipelined packet protocol. For support of the pipelined packet protocol he references col. 2, lines 34 et seq. and col. 20, line 6.

Katayama describes a storage device as a dynamic random access memory (DRAM). Each of Katayama's "memory systems" can carry out data reads or writes in a constant and short access time regardless of the timing with which the reads or writes, or refreshing are executed. Katayama also provides a method for controlling a DRAM that enables data reads or writes in a constant and short access time regardless of the timing with which the data reads or writes are executed. Applicant respectfully submits that the structure discussed in Katayama is just a variant of the DRAM devices used in Applicant's system.

In addition, the Examiner states that Katayama teaches a plurality of memory devices. For support, the Examiner points to the memory arrays, labeled 22, within the memory devices.

In contrast to Katayama, Applicant teaches a memory system having a plurality of N memory subsystems, wherein each subsystem contains a plurality M of memory devices. Each of these M memory devices could be implemented with DRAM devices. Each of these M memory devices could also be implemented with memory devices such as described by Katayama. The present teaching is significantly different from Katayama; Katayama only teaches a type of memory device which would fit within the memory device shown in Applicant's memory subsystem.

Katayama does not teach a plurality of memory subsystems with each memory subsystem having a plurality of memory devices as recited in the claims. Applicant respectfully notes that

Katayama. does not teach or suggest each and every feature of the present invention as claimed in independent claim 5. Accordingly, applicant asserts that claim 5 is allowable over Katayama.

Applicant further notes that Katayama's storage device does contain a data buffer and row and column decoder buffers. The Examiner correctly states that the row and column decode buffers correspond to an address buffer. Applicant's memory system contains one or more memory subsystems. Each subsystem includes a plurality of memory devices, a command buffer coupled between the command and address bus and the plurality of memory devices, and a data buffer connected between the plurality of memory devices and the bidirectional data bus. As would be well known to one skilled in the art Applicant's memory devices also contain a data in and a data out buffer, a column decoder and a row decoder. These structures are in addition to the command buffer coupled between the command and address bus and the plurality of memory devices, and the data buffer connected between the plurality of memory devices and the bidirectional data bus within the memory subsystem. These differences patentably distinguish the present claim 5 over Katayama.

The Examiner states that Katayama teaches pipelined packet protocol (Col. 2, lines 34 et seq and Col. 20, line 6). Katayama describes processing being operated in a pipelined manner where each time a data read is requested, the clock generator executes address latch, and then allows row decoding and column decoding, an array access, data transfer, and precharging to be sequentially carried out. (Col. 19, lines 66-67 and Col. 20, lines 1-7). Katayama discusses the pipelined manner in reference to how the processing is carried out when a data read is requested within the DRAM.

In contrast, Applicant refers to the memory subsystems within the memory system claimed as being pipelined. (Page 3, lines 16-17) The pipeline taught by Applicant is the sequence of data and address packets transmitted across the respective busses. (Page 9, lines 5-7) Both "packet" and "pipeline" are terms of art. Packet is a generic term for a bundle of data organized in a specific way for transmission. (Harry Newton, 13th Updated & Expanded Edition of Newton's Telecom Dictionary (1998)) Pipeline refers to overlapping operations by moving data or instructions into a conceptual pipe with all states of the pipe processing simultaneously. (Alan Freedman, The Computer Glossary (1995).) Both Katayama and the Applicant are using the word pipeline as a term of art to describe different operations within their inventions. In

addition, Applicant is using packet to describe bundles of data organized in a specific way for transmission.

The Examiner further states that

> It would have been obvious to one of ordinary skill in the art at the time the invention was made to include data in and data out buffers for each of the memory devices 22 in Katayama et al. system, since these buffers would have made the timing of the transfer operations to and from the shared buffers more efficient (by latching the data, control or address bits so that such protocols as time sharing could be utilized), especially considering the highly parallel nature of the Figure 9 embodiment of the Katayama et al. system.

However, this asserted motivation to modify Katayama in order to reject the present claims is essentially one of the benefits of the present invention. More specifically, the present invention uses the described structure and pipelined, packeted protocols, so that memory size can be increased without increasing the number of traces to form the required busses. Accordingly, transfer operations are more efficient. Applicant respectfully submits that the examiner's stated motivation for modifying Katayama is one contained in the present disclosure. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The Examiner must avoid hindsight. In re Bond, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). Withdrawal of the obviousness rejection is respectfully requested.

The Examiner rejected the claims based only on Katayama. Applicant respectfully traverses the single reference rejection under 35 U.S.C. § 103 since not all of the recited elements of the claims are found Katayama. Since all the elements of the claims are not found in the Katayama, Applicant assumes that the Examiner is taking official notice of the missing elements. Applicant respectfully objects to the taking of Official Notice with a single reference obviousness rejection and, pursuant to M.P.E.P. § 2144.03, Applicant respectfully traverses the assertion of Official Notice and requests that the Examiner cite references in support of this position.

Based at least on the above, applicant respectfully submits that claim 5 and claims 6-8